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EXAMINER	
HUBER, ROBERT T	

ART UNIT	PAPER NUMBER
2892	

NOTIFICATION DATE	DELIVERY MODE
09/22/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mweipdocket@mwe.com

Office Action Summary	Application No.	Applicant(s)	
	10/580,346	NAMBA ET AL.	
	Examiner	Art Unit	
	ROBERT HUBER	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-5,8,11-15 and 17-25* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-5,8,11-15 and 17-25* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *25 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. The Examiner acknowledges the amendment(s) to claim 8 filed on July 6, 2011. The objection(s) to claim 8 cited in the previous office action filed on March 10, 2011 is (are) hereby withdrawn.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1 – 5, 11 and 13 – 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida (US 6,340,393 B1, prior art of record) in view of Hasegawa et al. (US 2002/0127405 A1, prior art of record).

a. Regarding claim 1, **Yoshida discloses a diamond n-type semiconductor** (e.g. as seen in figure 3, and disclosed in col. 6, lines 18 - 20 to be n-type diamond) **comprising:**

a first diamond semiconductor which has n-type conduction (e.g. first diamond semiconductor 3, disclosed in col. 6, lines 18 – 20 to be n-type) **and in which a distortion or defect is artificially formed** (as disclosed in Yoshida, the n-type layer is doped with dopants, and therefore a distortion is formed in the diamond semiconductor lattice due to the dopant impurities. Furthermore, the patentability of a product does not depend on the method of production. See MPEP 2113),

wherein said first diamond semiconductor contains at least one kind donor element of 5 x 10^{19} cm^{-3} or more ion total (e.g. Phosphorus donor element, with concentration of 1x10^{20} cm^{-3} or more, as disclosed in col. 5, lines 49 – 50 and col. 5, line 67, and table 1) **and an impurity element other than the donor element** (e.g. impurity element H, col. 5, line 50) , **the contained amount of the impurity element being lower than the total contained amount of the donor element** (e.g. col. 2, lines 57 – 62, col. 3, lines 5 – 10, and col. 5, lines 34 – 39 disclose forming the impurity (acceptor) and donor in the diamond semiconductor with an atomic density ratio of 1:2 or 1:3, such that the amount of impurity (acceptor) material is 2 - 3 times less than the donor material),

whereby said first diamond semiconductor has an electron concentration exhibiting a negative correlation with temperature, in a temperature range having a width of 100℃ or more and included within a temperature region from 0℃ to 300℃ (This is considered a statement of device properties. See comment below),

wherein the donor element includes phosphorous (P) (e.g. as stated in col. 5, line 48), **and the impurity element having a contained amount of 1 x 10^{17} cm^{-3} or more** (e.g. col. 5, lines 34 - 39 discloses the ratio of atomic density of the p-type dopant (i.e. acceptor, impurity) to the n-type dopant (i.e. donor) should be 1:2 or 1:3. Since Yoshida discloses the n-type dopant to have an impurity of concentration of $1x10^{20}$ cm^{-3} in col. , line 67, the Yoshida anticipates or renders obvious that the impurity (p-type dopant) should be 1/2 or 1/3 of the donor (n-type dopant), or at least $0.33 x10^{20}$ cm^{-3} or more) **and locally existing in said first diamond semiconductor** (e.g. as disclosed in col. 5, lines 48 – 54, the impurity (e.g. p-type dopant H) is simultaneously formed with the first diamond semiconductor 3, therefore it is locally existing in the first diamond semiconductor) **as a material for restraining the deterioration of diamond crystallinity caused by the doping of the donor element** (This is considered a statement of device properties, or functional language. See comment below), **and**

wherein both P and the impurity element are incorporated during vapor-phase growth of said first diamond semiconductor (e.g. as disclosed

in col. 2, lines 49 – 52 and col. 5, lines 48 – 50. Furthermore, the patentability of a product does not depend on the method of production. See MPEP 2113).

Yoshida is silent with respect to disclosing the impurity element includes silicon (Si). Yoshida does disclose the impurity element (i.e. acceptor) to be a p-type dopant (e.g. col. 2, lines 51 – 52).

Hasegawa discloses that silicon can be used as a p-type impurity element when doping semiconductor diamond (¶ [0037] – [0038]).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Yoshida such that the impurity element is silicon since Yoshida discloses that the impurity element is a p-type dopant, and Hasegawa discloses that silicon can be used as p-type dopants in diamond semiconductors. Furthermore, it has been held that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. See MPEP 2144.07. One would be motivated to use silicon as an impurity element since it was a commonly used element in the semiconductor industry and is readily available with well-known properties, and one skilled in the art may adjust the band-gap and electrical properties of the semiconductor to using Si to optimize the semiconductor properties, such as conductivity, for a desired circuit, as discussed by Hasegawa (¶ [0037]).

Regarding the limitation "*said first diamond semiconductor has an electron concentration exhibiting a negative correlation with temperature, in a temperature range having a width of 100°C or more and included within*

***a temperature region from 0°C to 300°C*"**, **this is considered a property of the device, since it is the result of the structure of the device. The prior art of Yoshida in view of Hasegawa discloses the claimed structure, and it has been held that when the prior art discloses the structure of the claimed invention, a prima facie case of anticipation or obviousness of the properties of the device has been established. See MPEP 2112.01.**

Regarding the limitation of the silicon (Si) impurity "*as a material for restraining the deterioration of diamond crystallinity caused by the doping of the donor element*", the examiner finds this to be a statement of intended use or device properties. Since the device of Yoshida in view of Hasegawa discloses the claimed structure (i.e. diamond semiconductor doped with a donor element P and an impurity element Si), it is rendered obvious that the impurity element will restrain the deterioration of the diamond crystallinity. It has been held that when the prior art discloses the structure of the claimed invention, a prima facie case of anticipation or obviousness of the properties of the device has been established. See MPEP 2112.01.

For claims 2 – 5, see comment at end of section:

i. Claim 2, **Yoshida in view of Hasegawa disclose a diamond n-type semiconductor according to claim 1, as cited above, wherein said first diamond semiconductor has a Hall coefficient exhibiting a**

positive correlation with temperature, in the temperature range (see comment below)

ii. Claim 3, **Yoshida in view of Hasegawa disclose a diamond n-type semiconductor according to claim 1, as cited above, wherein the temperature range included within the temperature region from 0℃ to 300℃ has a width of over 200℃ or more** (see comment below)

iii. Claim 4, **Yoshida in view of Hasegawa disclose a diamond n-type semiconductor according to claim 1, as cited above, wherein said first diamond semiconductor has a resistivity of 500 Ωcm or less at a temperature within the temperature region from 0℃ to 300℃** (see comment below)

iv. Claim 5, **Yoshida in view of Hasegawa disclose a diamond n-type semiconductor according to claim 1, as cited above, wherein the electron concentration of said first diamond semiconductor is always 10^{16} cm^{-3} or more in the temperature region from 0℃ to 300℃** (see comment below)**.**

Regarding claims 2 – 5, the device of example shown in figure 3 of Yoshida contains an n-type diamond semiconductor layer containing a Phosphorus dopant concentration and a p-type impurity concentration, as

disclosed in col. 5, lines 48 - 54 and Table 1, which resides on a diamond substrate 2, as seen in figure 1. Since the device of Yoshida in view of Hasegawa meets the structural limitations of the claimed invention of the Applicant, the properties of the applicant's invention, such as the temperature dependence of the electron concentration and Hall coefficient as claimed in claims 2 - 5, are anticipated or rendered obvious to the device of Yoshida in view of Hasegawa. See MPEP 2112.01.

b. Regarding claim 11, **Yoshida in view of Hasegawa disclose a diamond n-type semiconductor according to claim 1, wherein said first diamond semiconductor is monocrystal diamond** (Yoshida: e.g. col. 2, line 49 – 50 disclose the first diamond semiconductor to be a single crystal (i.e. monocrystal) diamond thin film).

c. Regarding claim 13, **Yoshida in view of Hasegawa disclose a semiconductor device at least partly employing a diamond n-type semiconductor according to claim 1** (Yoshida: as disclosed in col. 6, lines 20 – 25).

d. Regarding claim 14, **Yoshida in view of Hasegawa disclose the diamond n-type semiconductor according to claim 1, as cited above,**

employed in at least an electron emitting part of an electron emitting device (Yoshida: col. 5, lines 18 – 19).

e. Regarding claim 15, **Yoshida in view of Hasegawa disclose a method of manufacturing a diamond n-type semiconductor according to claim 1, as cited above, said method comprising the steps of:**

preparing a diamond substrate (Yoshida: substrate 2, seen in figure 3 to be diamond and disclosed in col. 5, lines 43 - 44); **and**

epitaxially growing a diamond semiconductor on said diamond substrate by vapor phase growth (Yoshida: col. 4, lines 7 – 10, col. 4, lines 35 – 56 disclose forming the diamond semiconductor 3 by MOCVD (chemical vapor deposition) and MBE (molecular beam epitaxy), which forms the diamond semiconductor epitaxially from a vapor (gas) phase growth, as further disclosed in col. 2, lines 49 - 51) **while artificially introducing an impurity element other than a donor element to said diamond substrate** (Yoshida: e.g. col. 4, lines 47 - 52 discloses introducing an impurity element (acceptor) other than a donor element to (at) said diamond substrate), **whereby said diamond semiconductor has n-type conduction** (Yoshida: col. 6, lines 18 - 20 disclosed the diamond semiconductor 3 to be n-type diamond) **and has a distortion or defect which is artificially formed therein** (as disclosed in Yoshida, the n-type semiconductor layer 3 is doped with dopants (P) and impurities (acceptors H),

and therefore a distortion is formed in the diamond semiconductor lattice due to the impurities and dopants).

Yoshida is silent with respect to disclosing the impurity element is Si (silicon). Yoshida does disclose the impurity element (i.e. acceptor) to be a p-type dopant (e.g. col. 2, lines 51 – 52).

Hasegawa discloses that silicon can be used as a p-type impurity element when doping semiconductor diamond (¶ [0037] – [0038]).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Yoshida such that the impurity element is silicon since Yoshida discloses that the impurity element is a p-type dopant, and Hasegawa discloses that silicon can be used as p-type dopants in diamond semiconductors. Furthermore, it has been held that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. See MPEP 2144.07. One would be motivated to use silicon as an impurity element since it was a commonly used element in the semiconductor industry and is readily available with well-known properties, and one skilled in the art may adjust the band-gap and electrical properties of the semiconductor to using Si to optimize the semiconductor properties, such as conductivity, for a desired circuit, as discussed by Hasegawa (¶ [0037]).

5. Claims 8, 17 – 21 and 23 – 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida (US 6,340,393 B1, prior art of record) in view of Hasegawa

et al. (US 2002/0127405 A1, prior art of record) and Imai et al. (US 5,001,452, prior art of record).

a. Regarding claim 8, **Yoshida discloses a diamond n-type semiconductor** (e.g. as seen in figure 3, and disclosed in col. 6, lines 18 - 20 to be n-type diamond) **comprising:**

a first diamond semiconductor which has n-type conduction (e.g. first diamond semiconductor 3, disclosed in col. 6, lines 18 – 20 to be n-type) **and in which a distortion or defect is artificially formed** (as disclosed in Yoshida, the n-type layer is doped with dopants, and therefore a distortion is formed in the diamond semiconductor lattice due to the dopant impurities. Furthermore, the patentability of a product does not depend on the method of production. See MPEP 2113),

wherein said first diamond semiconductor contains at least one kind donor element of 5 x 10^{19} cm^{-3} or more ion total (e.g. Phosphorus donor element, with concentration of 1x10^{20} cm^{-3} or more, as disclosed in col. 5, lines 49 – 50 and col. 5, line 67, and table 1) **and an impurity element other than the donor element** (e.g. impurity element H, col. 5, line 50) , **the contained amount of the impurity element being lower than the total contained amount of the donor element** (e.g. col. 2, lines 57 – 62, col. 3, lines 5 – 10, and col. 5, lines 34 – 39 disclose forming the impurity (acceptor) and donor in the diamond semiconductor with an atomic density ratio of 1:2 or 1:3, such that the

amount of impurity (acceptor) material is 2 - 3 times less than the donor material),

whereby said first diamond semiconductor has an electron concentration exhibiting a negative correlation with temperature, in a temperature range having a width of 100℃ or more and included within a temperature region from 0℃ to 300℃ (This is considered a statement of device properties. See comment below),

wherein the impurity element having a contained amount of 1 x 10^{17} cm^{-3} or more (e.g. col. 5, lines 34 - 39 discloses the ratio of atomic density of the p-type dopant (i.e. acceptor, impurity) to the n-type dopant (i.e. donor) should be 1:2 or 1:3. Since Yoshida discloses the n-type dopant to have an impurity of concentration of $1x10^{20}$ cm^{-3} in col. , line 67, the Yoshida anticipates or renders obvious that the impurity (p-type dopant) should be 1/2 or 1/3 of the donor (n-type dopant), or at least $0.33 x10^{20}$ cm^{-3} or more) **and locally existing in said first diamond semiconductor** (e.g. as disclosed in col. 5, lines 48 – 54, the impurity (e.g. p-type dopant H) is simultaneously formed with the first diamond semiconductor 3, therefore it is locally existing in the first diamond semiconductor) **as a material for restraining the deterioration of diamond crystallinity caused by the doping of the donor element** (This is considered a statement of device properties, or functional language. See comment below), **and**

wherein both donor element and the impurity element are incorporated during vapor-phase growth of said first diamond semiconductor (e.g. as disclosed in col. 2, lines 49 – 52 and col. 5, lines 48 – 50. Furthermore, the patentability of a product does not depend on the method of production. See MPEP 2113).

Yoshida is silent with respect to disclosing wherein said first diamond semiconductor contains at least S (sulfur) as the donor element. As cited above, Yoshida discloses the donor element to be n-type (e.g. col. 2, lines 61 discloses the n-type dopant to be P, and col. 4, line 47 discloses the dopant P to be the donor).

Imai discloses a diamond n-type semiconductor (e.g. as disclosed in col. 4, lines 38 - 4) **contains at least S (sulfur) as the donor element** (e.g. as disclosed in col. 2, lines 20 – 23 and col. 4, line 68. Furthermore, col.2, lines 20 – 23 discloses that S (sulfur) may be substituted for P (phosphorus) as a dopant in n-type diamond semiconductors (col. 5, lines 7 – 10)).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Yoshida such that the donor element is sulfur since Yoshida discloses that the donor element is an n-type dopant, such as phosphorus, and Imai discloses that sulfur can be used as a substitute for phosphorus an n-type dopants in diamond semiconductors. Furthermore, it has been held that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. See

MPEP 2144.07. One would be motivated to use sulfur as a donor element since it was a commonly used element in the semiconductor industry and is readily available with well-known properties, and one skilled in the art may adjust the band-gap and electrical properties of the semiconductor to using sulfur to optimize the semiconductor properties, such as conductivity, for a desired circuit.

Yoshida is also silent with respect to disclosing the impurity element includes silicon (Si). Yoshida does disclose the impurity element (i.e. acceptor) to be a p-type dopant (e.g. col. 2, lines 51 – 52).

Hasegawa discloses that silicon can be used as a p-type impurity element when doping semiconductor diamond (¶ [0037] – [0038]).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Yoshida such that the impurity element is silicon since Yoshida discloses that the impurity element is a p-type dopant, and Hasegawa discloses that silicon can be used as p-type dopants in diamond semiconductors. Furthermore, it has been held that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. See MPEP 2144.07. One would be motivated to use silicon as an impurity element since it was a commonly used element in the semiconductor industry and is readily available with well-known properties, and one skilled in the art may adjust the band-gap and electrical properties of the semiconductor to using Si to optimize the semiconductor properties, such as conductivity, for a desired circuit, as discussed by Hasegawa (¶ [0037]).

Regarding the limitation "*said first diamond semiconductor has an electron concentration exhibiting a negative correlation with temperature, in a temperature range having a width of 100°C or more and included within a temperature region from 0°C to 300°C*", this is considered a property of the device, since it is the result of the structure of the device. The prior art of Yoshida in view of Imai and Hasegawa discloses the claimed structure, and it has been held that when the prior art discloses the structure of the claimed invention, a prima facie case of anticipation or obviousness of the properties of the device has been established. See MPEP 2112.01.

Regarding the limitation of the silicon (Si) impurity "*as a material for restraining the deterioration of diamond crystallinity caused by the doping of the donor element*", the examiner finds this to be a statement of intended use or device properties. Since the device of Yoshida in view of Imai and Hasegawa discloses the claimed structure (i.e. diamond semiconductor doped with a donor element S and an impurity element Si), it is rendered obvious that the impurity element will restrain the deterioration of the diamond crystallinity. It has been held that when the prior art discloses the structure of the claimed invention, a prima facie case of anticipation or obviousness of the properties of the device has been established. See MPEP 2112.01.

For claims 17 – 20, see comment at end of section:

v. Claim 17, **Yoshida in view of Imai and Hasegawa disclose a diamond n-type semiconductor according to claim 8, as cited above, wherein said first diamond semiconductor has a Hall coefficient exhibiting a positive correlation with temperature, in the temperature range** (see comment below)

vi. Claim 18, **Yoshida in view of Imai and Hasegawa disclose a diamond n-type semiconductor according to claim 8, as cited above, wherein the temperature range included within the temperature region from 0℃ to 300℃ has a width of over 200℃ or more** (see comment below)

vii. Claim 19, **Yoshida in view of Imai and Hasegawa disclose a diamond n-type semiconductor according to claim 8, as cited above, wherein said first diamond semiconductor has a resistivity of 500 Ωcm or less at a temperature within the temperature region from 0℃ to 300℃** (see comment below)

viii. Claim 20, **Yoshida in view of Imai and Hasegawa disclose a diamond n-type semiconductor according to claim 8, as cited above, wherein the electron concentration of said first diamond**

semiconductor is always 10^{16} cm^{-3} or more in the temperature region from 0℃ to 300℃ (see comment below)**.**

Regarding claims 17 – 20, the device of example shown in figure 3 of Yoshida contains an n-type diamond semiconductor layer containing a n-type donor concentration and a p-type impurity concentration, as disclosed in col. 5, lines 48 - 54 and Table 1, which resides on a diamond substrate 2, as seen in figure 1. Since Imai and Hasegawa teach the donor and impurity elements, and the device of Yoshida in view of Imai and Hasegawa meets the structural limitations of the claimed invention of the Applicant, the properties of the applicant's invention, such as the temperature dependence of the electron concentration and Hall coefficient as claimed in claims 17 – 20, are anticipated or rendered obvious to the device of Yoshida in view of Imai and Hasegawa. See MPEP 2112.01.

b. Regarding claim 21, **Yoshida in view of Imai and Hasegawa disclose a diamond n-type semiconductor according to claim 8, wherein said first diamond semiconductor is monocrystal diamond** (Yoshida: e.g. col. 2, line 49 – 50 disclose the first diamond semiconductor to be a single crystal (i.e. monocrystal) diamond thin film).

c. Regarding claim 23, **Yoshida in view of Imai and Hasegawa disclose a semiconductor device at least partly employing a diamond n-type**

semiconductor according to claim 8 (Yoshida: as disclosed in col. 6, lines 20 – 25).

d. Regarding claim 24, **Yoshida in view of Imai and Hasegawa disclose the diamond n-type semiconductor according to claim 8, as cited above, employed in at least an electron emitting part thereof** (Yoshida: col. 5, lines 18 – 19).

e. Regarding claim 25, **Yoshida in view of Imai and Hasegawa disclose a method of manufacturing a diamond n-type semiconductor according to claim 8, as cited above, said method comprising the steps of:**

preparing a diamond substrate (Yoshida: substrate 2, seen in figure 3 to be diamond and disclosed in col. 5, lines 43 - 44); **and**

epitaxially growing a diamond semiconductor on said diamond substrate by vapor phase growth (Yoshida: col. 4, lines 7 – 10, col. 4, lines 35 – 56 disclose forming the diamond semiconductor 3 by MOCVD (chemical vapor deposition) and MBE (molecular beam epitaxy), which forms the diamond semiconductor epitaxially from a vapor (gas) phase growth, as further disclosed in col. 2, lines 49 - 51) **while artificially introducing an impurity element other than a donor element to said diamond substrate** (Yoshida: e.g. col. 4, lines 47 - 52 discloses introducing an impurity element (acceptor) other than a donor element to (at) said diamond substrate), **whereby said diamond**

semiconductor has n-type conduction (Yoshida: col. 6, lines 18 - 20 disclosed the diamond semiconductor 3 to be n-type diamond) **and has a distortion or defect which is artificially formed therein** (as disclosed in Yoshida, the n-type semiconductor layer 3 is doped with dopants (P) and impurities (acceptors H), and therefore a distortion is formed in the diamond semiconductor lattice due to the impurities and dopants).

Yoshida is silent with respect to disclosing the impurity element is Si (silicon). Yoshida does disclose the impurity element (i.e. acceptor) to be a p-type dopant (e.g. col. 2, lines 51 – 52).

Hasegawa discloses that silicon can be used as a p-type impurity element when doping semiconductor diamond (¶ [0037] – [0038]).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Yoshida such that the impurity element is silicon since Yoshida discloses that the impurity element is a p-type dopant, and Hasegawa discloses that silicon can be used as p-type dopants in diamond semiconductors. Furthermore, it has been held that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. See MPEP 2144.07. One would be motivated to use silicon as an impurity element since it was a commonly used element in the semiconductor industry and is readily available with well-known properties, and one skilled in the art may adjust the band-gap and electrical properties of the

semiconductor to using Si to optimize the semiconductor properties, such as conductivity, for a desired circuit, as discussed by Hasegawa (¶ [0037]).

6. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida in view of Hasegawa, as applied to claim 1 above, and in further view of Shiomi et al. (US 5,252,840, prior art of record).

Yoshida in view of Hasegawa disclose a diamond n-type semiconductor according to claim 1, further comprising a second diamond substrate provided adjacent to said first diamond semiconductor (Yoshida: as seen in figure 3, second diamond substrate 2 is adjacent to the first diamond semiconductor 3).

Yoshida and Hasegawa are silent with respect to disclosing the second semiconductor is turned out to be n-type, wherein said second diamond semiconductor has an electron concentration exhibiting a negative correlation with temperature and a Hall coefficient not exhibiting a positive correlation with temperature, in the temperature range.

Shiomi discloses that a second diamond semiconductor may be provided adjacent to a first diamond semiconductor (e.g. figure 1(b), second diamond semiconductor 3, disclosed in col. 9, lines 46 – 48, adjacent to first diamond semiconductor 2, disclosed in col. 8, lines 21 - 22),

wherein said second diamond semiconductor has an electron concentration exhibiting a negative correlation with temperature and a Hall coefficient not exhibiting a positive correlation with temperature, in the

temperature range (col. 5, lines 16 – 24 disclose the structural characteristics of the device and layers. Since the device of Shiomi meets the structural limitations of the claimed invention of the Applicant, the properties of the applicant's invention, such as the temperature dependence of the electron concentration and Hall coefficient as claimed in claim 12, are presumed inherent to the device of Shiomi. See MPEP 2112.01).

Although Shiomi is silent with respect to the second semiconductor being n-type, Shiomi discloses the first and second diamond semiconductor layers to be p-type doped diamond semiconductor (col. 8, line 22 and col. 9, lines 46 - 49), **and it is well-known in the art that one may interchange p-type and n-type doping to achieve a desired charge carrier concentration of either holes or electrons** (e.g. as discussed in Shiomi, col. 1, lines 51 – 55). **One would have been motivated to substitute n-type doping for p-type doping in the first and second layers of Shiomi in order to create an n-type device, which would allow one to form complimentary circuits well-known in the semiconductor art (e.g. pn junctions).**

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Yoshida in view of Hasegawa such that a second diamond semiconductor layer was adjacent to the first diamond semiconductor layer, with the claimed properties, since Yoshida discloses a diamond substrate next to the first diamond semiconductor layer, and Shiomi discloses and renders obvious that one may form a second diamond semiconductor layer next to the first diamond semiconductor layer having the claimed structure. One would have been motivated to

form a second diamond semiconductor layer adjacent to the first diamond semiconductor layer in order to allow charge carrier diffusion from the first layer into the second layer, thereby altering the conduction properties of the device, as disclosed by Shiomi (col. 5, line 16 – 21).

7. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida in view of Imai and Hasegawa, as applied to claim 8 above, and in further view of Shiomi et al. (US 5,252,840, prior art of record).

Yoshida in view of Imai and Hasegawa disclose a diamond n-type semiconductor according to claim 8, further comprising a second diamond substrate provided adjacent to said first diamond semiconductor (Yoshida: as seen in figure 3, second diamond substrate 2 is adjacent to the first diamond semiconductor 3).

Yoshida, Imai and Hasegawa are silent with respect to disclosing the second semiconductor is turned out to be n-type, wherein said second diamond semiconductor has an electron concentration exhibiting a negative correlation with temperature and a Hall coefficient not exhibiting a positive correlation with temperature, in the temperature range.

Shiomi discloses that a second diamond semiconductor may be provided adjacent to a first diamond semiconductor (e.g. figure 1(b), second diamond semiconductor 3, disclosed in col. 9, lines 46 – 48, adjacent to first diamond semiconductor 2, disclosed in col. 8, lines 21 - 22),

wherein said second diamond semiconductor has an electron concentration exhibiting a negative correlation with temperature and a Hall coefficient not exhibiting a positive correlation with temperature, in the temperature range (col. 5, lines 16 – 24 disclose the structural characteristics of the device and layers. Since the device of Shiomi meets the structural limitations of the claimed invention of the Applicant, the properties of the applicant's invention, such as the temperature dependence of the electron concentration and Hall coefficient as claimed in claim 12, are presumed inherent to the device of Shiomi. See MPEP 2112.01).

Although Shiomi is silent with respect to the second semiconductor being n-type, Shiomi discloses the first and second diamond semiconductor layers to be p-type doped diamond semiconductor (col. 8, line 22 and col. 9, lines 46 - 49), **and it is well-known in the art that one may interchange p-type and n-type doping to achieve a desired charge carrier concentration of either holes or electrons** (e.g. as discussed in Shiomi, col. 1, lines 51 – 55). **One would have been motivated to substitute n-type doping for p-type doping in the first and second layers of Shiomi in order to create an n-type device, which would allow one to form complimentary circuits well-known in the semiconductor art (e.g. pn junctions).**

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Yoshida in view of Imai and Hasegawa such that a second diamond semiconductor layer was adjacent to the first diamond semiconductor layer, with the claimed properties, since Yoshida discloses a diamond

substrate next to the first diamond semiconductor layer, and Shiomi discloses and renders obvious that one may form a second diamond semiconductor layer next to the first diamond semiconductor layer having the claimed structure. One would have been motivated to form a second diamond semiconductor layer adjacent to the first diamond semiconductor layer in order to allow charge carrier diffusion from the first layer into the second layer, thereby altering the conduction properties of the device, as disclosed by Shiomi (col. 5, line 16 – 21).

Response to Arguments

8. Applicant's arguments filed July 6, 2011 have been fully considered but they are not persuasive. The Applicants argue that the prior art of Hasegawa cannot be combined with Yoshida since the acceptor "H" of Yoshida cannot be replaced by "Si", as taught by Hasegawa. The Applicants assert that if "H" of Yoshida is replaced with "Si", then the donor-acceptor compound cannot be formed because "Si" is a Group 4 element, and silicon carbide will formed and localize in the diamond crystal, which will result in a compound with properties that are not the intended purpose and objective of Yoshida (see pages 9 – 10 of Remarks). The Examiner respectfully disagrees. Yoshida clearly states that the diamond semiconductor may be formed by simultaneously doping the doping with both an n-type and p-type dopant (e.g. see col. 2, lines 49 – 56, col. 4, lines 62 – 67, etc..), and Yoshida states that the p-type dopant can be hydrogen (H) (e.g. col. 2, line and col. 4, line 49 - 50). The Examiner acknowledges that Yoshida does not teach the p-type dopant to be Si, however Yoshida explicitly teaches using a p-type

dopant in order to stabilize the n-type dopant in high densities (col. 2, lines 51 - 56). Although Yoshida teaches the use of H as the p-type dopant (e.g. acceptor), the invention of Yoshida is to the simultaneous doping of n-type and p-type dopants, and nowhere does Yoshida teach that other materials cannot be used for the p-type dopant. The Examiner submits that one of ordinary skill in the art would recognize from the disclosure of Yoshida that other p-type materials may be used in order to help stabilize the high density n-type dopant concentrations. Since Yoshida discloses the use of a p-type dopant for such a material in diamond substrates, and Hasegawa teaches the use of Si as a p-type material in diamond substrates, the Examiner submits that one of ordinary skill in the art would recognize to substitute the p-type dopant Si for the p-type dopant H.

9. Furthermore, the Attorney's argument against the substitution of Si, as taught by Hasegawa, for the acceptor H, as taught by Yoshida, may be regarded as speculation since it has not been shown conclusively that substituting Si for H cannot be made, and that substituting Si for H will result in an inoperable device, and an argument by an Attorney is not the kind of factual evidence that is required to rebut a prima facie case of obviousness. See MPEP 2145. The Examiner submits that one of ordinary skill in the art will recognize that Si may be substituted for H in Yoshida, since Yoshida discloses the use of a p-type dopant for offsetting the n-type dopants in the diamond semiconductor substrate, and Hasegawa teaches Si to be a useful p-type dopant in diamond semiconductor substrates.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT HUBER whose telephone number is (571)270-3899. The examiner can normally be reached on Monday - Friday (11am - 7pm EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lex Malsawma/
Primary Examiner, Art Unit 2892

/Robert Huber/
Examiner, Art Unit 2892
September 12, 2011